REMARKS/ARGUMENTS

Claims 1-12, 14-28 are now pending. No claims stand allowed.

Claim 13 has been canceled, without prejudice.

Claims 1, 4-12, 17-18, 20-21, and 24-27 have been amended to further particularly point out and distinctly claim subject matter regarded as the invention. The text of claims 2-3, 14-16, 19, and 22-23 remain unchanged, but their meaning is changed because they depend from amended claims. New claim 28 has been added by this amendment and also particularly point out and distinctly claim subject matter regarded as the invention. The amendment also contains minor changes of a clerical nature. No "new matter" has been added by the amendment.

Claim Objections

Claims 9-27 stand objected to because of certain minor informalities in claims 9, 12-13, and 20-21. The claims have been amended to correct the minor informalities in accordance with the Examiners suggestion. With this amendment, it is respectfully requested that the objection to the claims be withdrawn.

The 35 U.S.C. §102 Rejection

Claims 1, 3, and 6-8 stand rejected under 35 U.S.C. §102(b) as being allegedly anticipated by Moore et al. (U.S. Pat. No. 5,437,017), among which claims 1 and 8 are independent claims. This rejection is respectfully traversed.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 869 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). *See also*, M.P.E.P. §2131.

Claim 1 defines a method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the processors having an associated TLB for storing address translation data, the system having a main communication network coupled to the plurality of processors. The claimed method includes, among others, (1) generating a TLB message in response to the operation performed on the first TLB, ... , the TLB message comprising an access request and the associated physical address; (2) sending the TLB message to the plurality of processors other than the processor associated with the first TLB via the main communication network; and (3) determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data in the associated TLB in response to receiving the TLB message.

The Examiner alleges that Moore discloses the method for maintaining TLB coherency. In the Office Action, the Examiner especially equates the translation lookaside buffer invalidate (TLBI) instruction of Moore with the TLB message of the claimed invention. However, the TLBI instruction and the response thereto in Moore's

system are different from and thus do not disclose the claimed invention for the following reasons.

Moore's system uses not only the "TLBI instruction" but also "TLBI bus structure" to ensure TLB coherency among the processors. As described in detail in column 7, line 2 to column 9, line 66 and FIGS. 4 and 5 of Moore, the TLBI instruction is first issued and executed locally (column 7, lines 2-36) based on a local memory event, and then a TLBI bus structure associated with the TLBI instruction which was just executed is broadcast onto the bus (column 7, lines 44-48). When the TLBI bus structure is received or accepted by other processors on the bus, nothing happens *in response to* such receipt or acceptance. However when the TLBI bus structure is NOT accepted by one or more other processors, a corresponding "RETRY" message is detected by the processor which initially executed the TLBI instruction (column 7, line 57 to column 8, line 5 of Moore). On the other hand, when the broadcast TLBI bus structure is detected or received by other processors, the receiving processor always checks to see if a "TLBI PENDING" has been set by a previous TLBI, and if so, it asserts a "RETRY" message (column 8, lines 39-56 of Moore). Then, the receiving processor further checks to see if any other processor is asserting a "RETRY" message (column 8, lines 57-68 of Moore). Furthermore, only after flagging a new "TLBI PENDING," the receiving processor starts executing the TLBI instruction, putting the instruction to the "EXECUTE" position (column 9, lines 1-29 of Moore).

Accordingly, if the TLBI instruction corresponds to the claimed TLB message as the Examiner alleges, although the TLBI instruction may be issued as a result of the relocation of data or any other operation which modifies the translation relationship between virtual and real addresses (column 7, lines 13-18 of Moore), the TLBI instruction is only executed in that local processor, and is not sent to other processors as claimed. In Moore, it is the TLB bus structure that is sent to the other processors. In addition, since the TLB bus structure is broadcast only after the execution of the TLBI instruction and arbitration to obtain access to the bus (see blocks 54, **56**, **58**, and **60** in FIG.4 of Moore), the TLB bus structure cannot be generated *in response to* the operation performed on the TLB, as claimed in claim 1.

Furthermore, as discussed above, when the TLB bus structure is received by the other processors, a series of processes (checking RETRY, checking outstanding TLBI PENDING, flagging TLBI PENDING) are performed in Moore, but there is no process to determine if the TLB bus structure (or alleged TLB message) affects the address translation data store in the TLB, as recited in claim 1. Accordingly, Moore also fails to disclose or teach determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the address translation data stored in the associated TLB in response to receiving the TLB message, as recited in claim 1.

Claim 8 includes substantially the same distinctive features as claim 1.

Accordingly, it is respectfully requested that the rejection of claims based on Moore be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

The 35 U.S.C. §103 Rejection

Claims 1 and 9-27 stand rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Chan et al. (U.S. Pat. No. 5,524,216) in view of Moore et al., among which claims 1, 8, 9, 12, and 20 are independent claims. This rejection is respectfully traversed.

According to M.P.E.P. §2143,

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in the applicant's disclosure.

As the Examiner correctly mentions in the Office Action, Chan fails to teach generating a TLB message which is transmitted to other TLBs within the system. The Examiner relies on Moore for these missing features. However, as discussed above in detail, Moore also fails to teach or suggest generating a TLB message which is transmitted to other TLBs within the system, and determining, at each of the plurality of processors other than that associated with the first TLB, if the TLB message affects the

address translation data stored in the associated TLB in response to receiving the TLB message, as recited in claim 1.

Claim 8, 9, 12, and 20, as amended, includes substantially the same distinctive features as claim 1, and thus the argument set forth above is equally applicable.

Accordingly, Chan, whether considered alone or combined with or modified by Moore, does not teach or suggest the claimed invention. It is respectfully requested that the rejection of claims based on Chan and Moore be withdrawn. In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Dependent Claims

Claims 2-7, 19, and 28 depend from claim 1, claim 10-11 depend from claim 9, claims 14-18 depend from claim 12, and claims 21-27 depend from claim 20, and thus include the limitations of respective independent claims. The argument set forth above is equally applicable here. The base claims being allowable, the dependent claims must also be allowable at least for the same reasons.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Request for Allowance

It is believed that this Amendment places the above-identified patent application

into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Respectfully submitted,
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Masako Ando
Limited Recognition under 37 CFR §10.9(b)

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